select signal to the first multiplexer.

Claim 48 Cancelled.

42 ~~49~~. (Previously Added) The system of Claim ~~48~~ 40, wherein the multi-gigabit transceiver comprises a phase locked loop configured to receive the clock signal selected by the first multiplexer.

43 ~~50~~. (Previously Added) The system of Claim ~~49~~ 42, wherein the multi-gigabit transceiver further comprises a serializer configured to operate in response to a serializing clock signal generated by the phase locked loop in response to the clock signal selected by the first multiplexer.

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44 ~~51~~. (Previously Added) The system of Claim ~~42~~ 36, wherein the programmable logic device further comprises:

a first general-purpose clock pad;

a first down-level shifter coupled to the first general-purpose clock pad; and

a general-purpose clock routing path coupling the down-level shifter to the multi-gigabit transceiver.

45 ~~52~~. (Previously Added) The system of Claim ~~51~~ 44, wherein the programmable logic device further comprises a multiplexer coupled to the dedicated routing structure and the general-purpose clock routing path, the multiplexer being configured to selectively route a clock signal on either the dedicated routing structure or the general-purpose clock routing path in response to a select signal.

46 ~~53~~. (Previously Added) The system of Claim ~~52~~ 45, wherein the programmable logic device further comprises a first configuration memory cell that is programmable to store and provide the select signal.

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